UNITED STATES PATENT AND TRADEMARK OFFICE

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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Application Number: 09/772,584
Filing Date: January 29, 2001
Appellant(s): SUBRAMANIAN ET AL.

Laura C. Brutman
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/13/2006 appealing from the Office action

mailed 11/5/2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,999,990   SHARRIT et al   12-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-16 and 51-66 are rejected under 35 U.S.C. 102(e) as being anticipated by

Sharrit et al., US patent No. 5,999,990.

- As to claims 1 and 51, Sharrit et al teach in a processor [communicator 10 in fig. 1]

  having a plurality of kernel planes [e.g., controller 16 and RRUs block 13 in figs. 1, 4,

  and 5] with a plurality of kernels [e.g., reconfigurable resources units (RRUs) 12a-

  12n in the RRUs block 13 in fig. 1] for processing data in a communication device

  [col. 2, lines 3-5], at least one kernel [e.g., RRU 12a in fig. 1] of the plurality of

  kernels comprising:

     an interface [signal bus 14 in fig. 1 and col. 2, lines 31-34] adapted to receive and

  transmit information from the at least one kernel;

     a satellite kernel [e.g., block including DSP (digital signal processor) 42 and RAM

  44 in fig. 2 or FPGA (field programmable gate array), DSP in figs. 3 and 4; col. 6,

  lines 23-29] coupled to the interface, the satellite kernel performing a discrete class

  of operations [col. 3, lines 13-22; col. 4, lines 58-61] within a communications

  application; and

     a local controller [DSP 42 in fig. 2 or GPP (general purpose processor) 48, 60 in

  figs. 3 and 4] coupled to the interface and the satellite kernel, and the local controller

  permitting the at least one kernel [RRU 12a] to operate autonomously [col. 5, lines

  41-43; col. 6, lines 14-22; col. 2, lines 35-43; col. 5, lines 8-14] with respect to the

  other [e.g., RRU 12b in fig. 1] of the plurality of kernels.

- As to claims 2 and 52, Sharrit et al teach the satellite kernel is configurable to perform a specific sub function within the class of sub functions [col. 5, lines 10-17].

- As to claims 3 and 53, Sharrit et al teach the satellite kernel is reconfigurable from a first sub function to perform a second sub function within the discrete class of operations [col. 7, lines 28-44; col. 6, lines 29-35].

- As to claims 4 and 54, Sharrit et al teach the satellite kernel is reconfigurable only within the class of operations [col. 2, lines 35-50].

- As to claims 5 and 55, Sharrit et al teach the satellite kernel includes a plurality of electronic devices for performing arithmetic, logic, and storage operations, the plurality of electronic devices coupled to each other and to the local controller in a fixed manner for implementing functions common to the class of operations, the plurality of electronic devices coupled to each other in a reconfigurable manner for implementing functions unique within the class of operations [col. 5, line 58-col. 6, line 13].

- As to claims 6 and 56, Sharrit et al teach the electronic devices are coupled to each other using a reconfigurable logic technique, a reconfigurable datapath technique, a reconfigurable dataflow technique, or a reconfigurable control technique for the discrete class of operations performed by the satellite kernel [col. 5, line 58-col. 6, line 13].

- As to claims 7 and 57, Sharrit et al teach the electronic devices are coupled to each other using a heterogeneous combination of the reconfigurable logic technique, the

reconfigurable datapath technique, the reconfigurable dataflow technique, or the

reconfigurable control technique [col. 5, line 58-col. 6, line 13].

- As to claims 8 and 58, Sharrit et al teach the reconfigurability of the at least one

  kernel is established on a temporal basis, a logical basis, or a functional basis [figs.

  6-7].

- As to claims 9 and 59, Sharrit et al teach the class of operations is based upon a

  desired level of performance for the application [col. 3, lines 23-35].

- As to claims 10 and 60, Sharrit et al teach the discrete class of operation is an

  algorithm [col. 8, lines 41-53].

- As to claims 11 and 61, Sharrit et al teach the class of operations is limited to a class

  of mathematical field operations [col. 8, lines 41-53].

- As to claims 12 and 62, Sharrit et al teach the application within which the

  operations are used is a wireless communications application [fig. 1].

- As to claims 13 and 63, Sharrit et al teach the operations used in the wireless

  communications application include modem operations and codec operations [col. 5,

  lines 18-32; col. 7, lines 15-27].

- As to claims 14 and 64, Sharrit et al teach the local controller manages the satellite

  kernel autonomously from circuitry outside [col. 4, lines 9-27].

- As to claims 15 and 65, Sharrit et al teach the satellite kernel includes a computing

  element at a lower hierarchical level than the satellite kernel [fig. 4].

- As to claims 16 and 66, Sharrit et al teach the satellite kernel includes a plurality of selective interconnects coupling the plurality of electronic devices [col. 5, line 58-col. 6, line 13].

(10) Response to Argument

The Examiner summarizes the various points raised by the Appellant and addresses replies individually.

a.   *The Appellant alleges that Sharrit does not teach or even suggest a kernel having a local controller that permits the kernel to operate autonomously with respect to other of the plurality of kernels (page 6, lines 13-15 of Appeal Brief).*

The Examiner respectfully disagrees with the Applicant's arguments.

The DSP 42 then reads the signal from the signal bus 14 and processes it by executing one or more software programs stored in RAM 44. [Sharrit: col. 5, lines 41-43]

With reference to FIG. 3, the GPP 48 is coupled to the controller 16 for receiving instructions on how to process a signal on bus 14. In response to the instructions, the GPP 48 delivers a control signal to FPGA 50 instructing it to read the signal on signal bus 14 and to process the signal in an appropriate area of the cell array. The GPP 48 can also receive configuration files from the controller 16 for use in reconfiguring the FPGA 50. GPP 48 then delivers the configuration files to a designated portion of FPGA 50. [Sharrit: col. 6, lines 14-22]

Each of the plurality of RRUs 13 includes signal processing functionality for processing signals on the signal bus 14. In accordance with the present invention, each of the RRUs can be dynamically altered in the field to change the processing functions they are configured to perform. That is, a particular RRU (e.g., RRU 12a) can be set up to perform one set of processing functions at one moment and a different set of processing functions at another moment, based on current system requirements. [Sharrit: col. 2, lines 35-43]

A particular receive signal on signal bus 14 may need to be processed in multiple RRUs before being delivered to a user at user device 40. In one embodiment, this processing is done in a sequential manner, where the signal is individually processed by separate RRUs one after the other. In another embodiment, multiple RRUs are linked together to process the signal in tandem. [Sharrit: col. 5, lines 8-14]

As seen above, Sharrit teaches each kernel [RRU (reconfigurable resources unit)] has its own local controller [e.g., DSP (digital signal <u>processor</u>) or GPP (general purpose <u>processor</u>)] and its own storage storing software programs. The local controller using its own software programs permits its kernel [e.g., RRU 12a] to operate autonomously its own functionality with respect to the other kernels [e.g., RRU 12b] having different functions.

b.   *The Appellant alleges that Sharrit has centralized control in its controller as opposed to the claimed distributed control. Sharrit's controller 16 MIPS rating and bus 14 width and speed rating limit the number of RRU's or the reconfiguration abilities versus time. With equal ratings for the controller and buses, the distributed control system of the claimed invention is more scaleable in that it can support more kernels or more reconfigurations per second that Sharrit (page 6, line15-page 7, line 2 of Appeal Brief).*

The Appellant further alleges that Sharrit's GPP is not equivalent to the claimed local controller; there is no suggestion in Sharrit that the GPP performs local controller functions. In order for the GPP to perform the local controller functions and do resource allocation, it would need to obtain information from the DSP and/or the FPGA (page 7, lines 3-9 of Appeal Brief).

The Appellant another further alleges that Sharrit system does not scale well as the number of RRU increases; on the other hand, the claimed kernel's local controller scales wells as the number of kernels increases (page 7, line 13-page 8, line 2 of Appeal Brief).

It is noted that the features upon which appellant relies (i.e., *centralized control or distributed control, equal ratings, scaleable supporting more kernels or more reconfigurations per second, reading information from anywhere in order to perform the local controller functions, local controller scales wells as the number of kernels increases*) are not recited in the rejected claims; although the claims are interpreted in the light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

When claim construction is required, claims are construable, as above indicated, in light of the specification, United States v. Adams, 383 U.S. 39, 49, 148 USPQ 479, 482 (1966), yet "[t]hat claims are interpreted in light of the specification does not mean that everything expressed in the specification must be read into all the claims." Raytheon Co. v. Roper Corp., 724 F.2d at 957, 220 USPQ at 597. If everything in the specification were required to be read into the claims, or if structural claims were to be limited to devices operated precisely as a specification-described embodiment is operated, there would be no need for claims. Nor could an applicant, regardless of the prior art, claim more broadly than that embodiment. Nor would a basis remain for the statutory necessity that an applicant conclude his specification with "claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
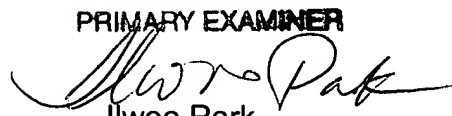
(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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